Digital Beamforming for Smart Antennas

Todd W. Nuteson and Gregory S. Mitchell

The Aerospace Corporation, Chantilly, VA, 20151

Abstract – An 8-channel digital phased array antenna (PAA) is designed and evaluated for a smart antenna [1] application in the cellular PCS band (1850 MHz to 1990 MHz). Each channel is digitized at the RF carrier frequency using bandpass sampling clocking up to 1.5 Gsps with a 140 MHz bandwidth. The beamforming and additional signal processing is implemented digitally using field programmable gate arrays (FPGAs). This paper characterizes the PAA system for effects on loading analog-to-digital converters (ADCs) including automatic gain control (AGC) techniques and co-channel interference.

1. Introduction

With current advances in high-speed ADC technology, it becomes feasible to digitize at the RF carrier frequency in the front-end of a PAA. This is very attractive because it leads to the elimination of the majority of analog RF hardware, including the analog receiver down-converter. In a typical analog PAA system, each antenna element passes through a low-noise amplifier (LNA), phase-shifter, and amplitude control block. The elements are then combined with an analog beamformer, which feeds the RF/IF receiver. In the receiver the RF signal is down-converted to IF and then digitized with a relatively slow ADC, usually with 8- to 12-bits of resolution. For a multichannel analog PAA, the hardware chain would have to be duplicated for each channel rendering the PAA complex, large, and very expensive. Reference [2] presents a PAA approach that implements digital beamforming where the ADCs are placed after each IF receiver. In a full-digital PAA approach, each antenna element would have an ADC behind it after the LNA as shown in Fig. 1. Here the RF signal is digitized directly using bandpass sampling [3] eliminating any need for an analog RF/IF receiver. The channels are then combined and configured in the digital domain using FPGAs or ASICs where amplitude and phase (or time delays) can be applied to each antenna element, to form the desired antenna beams. With digital signal processing it becomes less of a burden to implement adaptive antenna processing techniques [4], such as pattern nulling or space-time adaptive processing (STAP) [5]. With a large digital PAA, the required individual ADC resolution can be reduced to well under 8-bits; and in some cases 1-bit is adequate. Fig. 2 shows the signal-to-noise ratio (SNR) gain for up to 128 ADCs with resolutions of 1, 3, and 8 bits. SNR Gain is achieved by summing coherent signals and incoherent noise where the noise is assumed to be Gaussian. It should be pointed out that as ADC resolution is decreased, the SNR input to the ADC needs to be considered, due to the limited dynamic range of the ADC. For example, the 1-bit case is over driven with a 10 dB input SNR as is shown in Fig. 2. The primary performance driver in PAA systems is SNR. The noise term in the SNR expression contains a variety of components including thermal noise, quantization noise, intermod distortion, and interference (typically man-made co-channel interference). With the obvious objective to maximize SNR, the PAA has as its task to combine signals in such a way that the spatially diverse interference is reduced, and the remaining noise terms are optimally maintained at some minimal level. While many well known techniques exist for interference reduction via nulling or beam steering [1], there is yet no agreement as to the best approach for managing the remaining noise terms that arise in fully digital PAA implementation. In particular, full-digital PAA implementations differ from partial or analog implementations with respect to the noise and interference contributed to the system by the ADC. Managing this noise has been shown to be a function of the proper choice and operation of the ADC. In the following sections, we present the results of modeling and experimental efforts to characterize and address these issues and as well explore some of the powerful benefits of realizing full-digital PAA implementations.

2. Digital Phased Array Antenna System

Fig. 1 shows the architecture for the PAA system that was developed in this work. The system bandwidth is 140 MHz covering the cellular PCS band from 1850 MHz to 1990 MHz. It has 8 channels (N=8) with a linear, dipole antenna-array at the front-end followed by LNAs. The scanning performance of the antenna

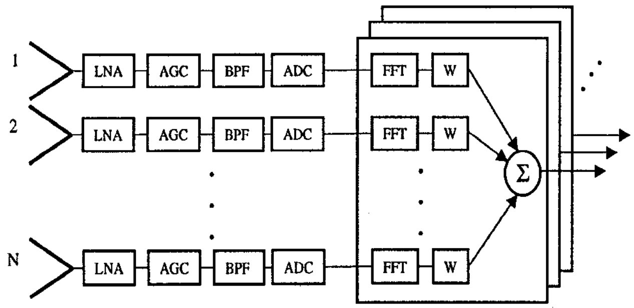

Figure 1: Digital phased array antenna system block diagram.

array is shown in Fig. 3. The LNAs have a 26 dB gain and a noise-figure of 1.2 dB. One of the most critical components in the system is the AGC, because loading the ADC is crucial to optimize the performance of the digital beamformer. The loading issues and AGC are discussed in the next sections. After the AGC, the signal is filtered and then sent into the ADC. The ADC is commercially available from Maxim (MAX108). It has an 8-bit resolution with a 1.5 Gsps clock rate. From Fig. 2, for an 8-bit system with 8 ADCs, the SNR gain is close to 9 dB. The digital beamforming is done in real-time using FPGAs from Xilinx. The FPGAs are programmed to compute the FFT of each channel which are then amplitude and phase weighted to simultaneously receive signals over a ±30 degree scan. Adaptive processing is currently being implemented for beam-nulling.

3. Analog-to-Digital Converter Loading

The fully-digital PAA suffers from an inherent degradation in SNR as a result of quantization and intermodulation distortion noise. It can be argued that the numerous benefits of the digital PAA will outweigh this cost, provided that the degradation can be managed at some minimum value. This ultimately requires optimal loading of the ADC. That is, on the one hand, it must be given an input voltage range that does not overload the ADC causing clipping of the signal, which, as in any system undergoing such a nonlinear operation, will result in spurious noise. On the other hand, the input voltage range cannot be too small, as to cause the ADC to be under utilized because the input range of the signal is so much smaller than the ADCs full scale range (FSR); in this case the quantization noise will be large. The spur-free dynamic-range (SFDR) for signal loading only (no noise) of the ADC is shown in Fig. 4.

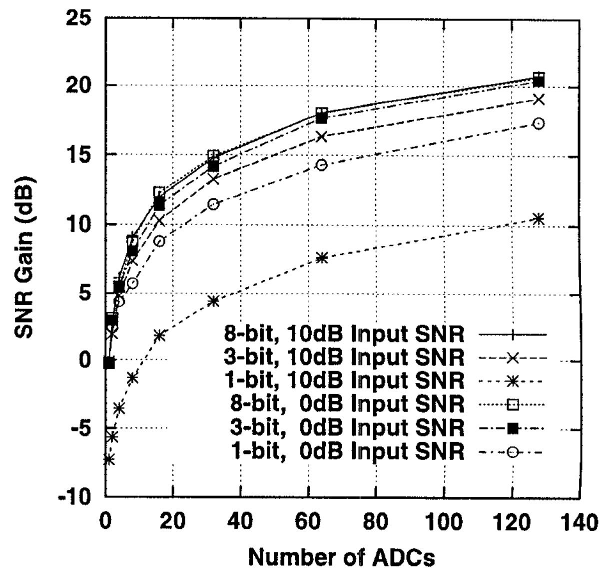

Figure 2: Simulated SNR gain for 1 to 128 channels.

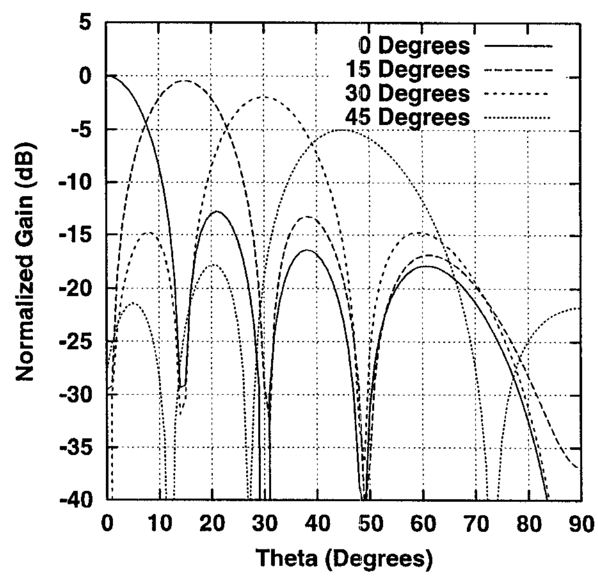

Figure 3: Simulated scanned antenna patterns of phased array antenna.

0-7803-6540-2/01/$10.00 (C) 2001 IEEE

It can be seen here that to maximize SFDR, overloading of the ADC is not recommended. Therefore some headroom should be allocated. Several loading conditions are shown in Fig. 5 for a broad range of input SNRs for the 8-bit, 8 ADC system. The results correspond to load factors of 20%, 40%, 60%, 80%, 100%, 150%, and 200% where the 20% load curve flattens out at 40 dB and the maximum load (200%) curve flattens out around 56 dB. The rest of the load curves fall in between respectively. Observations noticed here are overloading causes an overall output SNR degradation over the dynamic range of the system with more loss occurring as the input SNR decreases. On the other side, overloading appears to add a couple of dB in the saturated part of the curve; performance is dominated by quantization noise [6] in the ADCs. The effect of underloading the ADCs is not a loss in output SNR, but a loss in dynamic-range. The 100% load case has about 14 dB more of dynamic range when compared to the 20% load case.

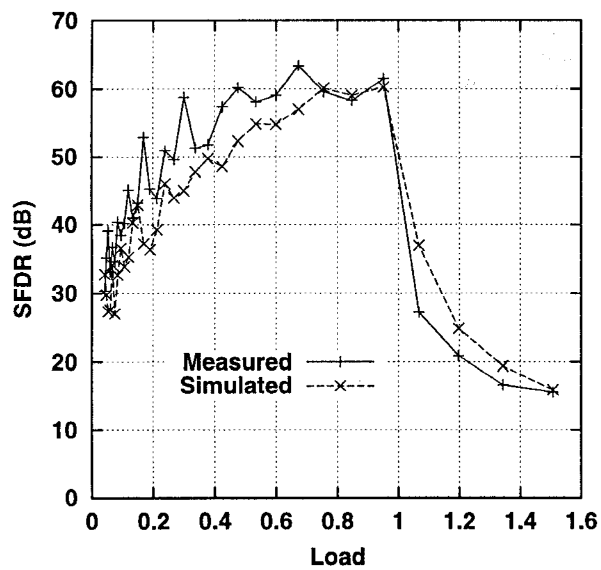

Figure 4: Spur-free dynamic-range versus loading for the 8-bit Maxim ADC.

4. Automatic Gain Control

Since appropriate loading of the ADC is crucial for good SFDR performance and system dynamic-range, an AGC is needed to control the power-levels into the ADCs. In traditional analog PAAs, there is usually only one ADC with an AGC after the IF receiver. For the system in this paper, there are 8 channels with 8 ADCs that need to have independent AGC control. Typically

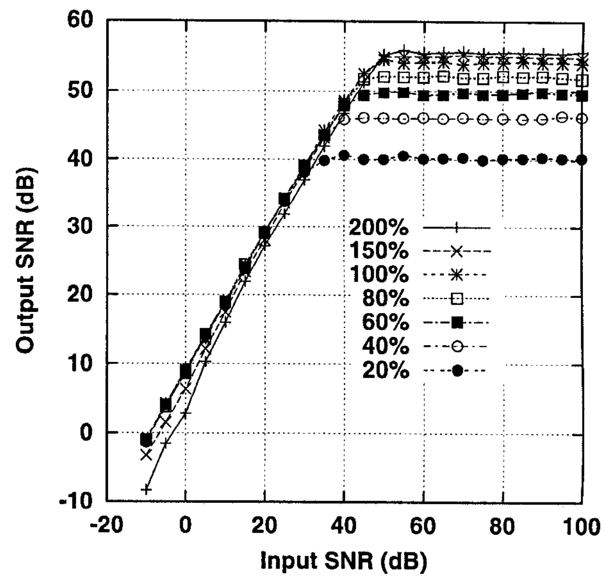

Figure 5: Simulated input SNR versus output SNR for several ADC load conditions. 8-bit, 8 ADC.

all the received amplitude levels in each channel would be the same, if there is no co-channel interference. With co-channel interference and multipath fading, the amplitude levels on each channel could vary significantly. There are two approaches that were considered to counteract this effect. The first approach searches for the peak signal in all 8 channels over an integrated time interval, and then sets one gain for all 8 channels to load the ADCs. With this approach, if the amplitude levels vary significantly, the loads for the ADCs will all be different. The second approach has an independent AGC on each channel and loads each ADC at full capacity (e.g. 95%). In this approach, if the amplitudes are different for each channel, the amplitude information is destroyed. To get back the amplitude information, the weights that were used for each channel need to be saved and used later in the digital processing. This approach is more complicated to implement in hardware but is realizable. Both AGC approaches are compared in Fig. 6 for the 3-bit and 8-bit cases with the 8-channel system. The 8-bit cases are the two curves that have more dynamic-range with the second AGC approach having about 3 dB more dynamic range over the first AGC approach. Similar results occur for the 3-bit cases. The second AGC approach (independent AGC per channel) has more dynamic range because it is optimally loading the ADC, which results in the minimum quantization noise possible.

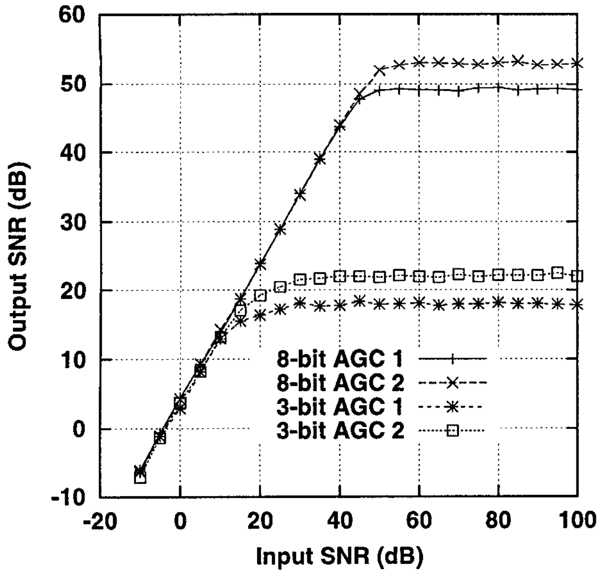

Figure 6: Simulated output SNR versus input SNR for both AGC approaches.

5. Co-Channel Interference

In a PCS environment, co-channel interference [7] is of great concern. The advantage of having a PAA is the capability of beam-steering and adaptive nulling. The half-power beamwidth of the PAA in this paper is 12.8 degrees. In this case, co-channel interference is only of concern when the interference is in or nearby the antenna beam of interest. The fully-digital PAA offers tremendous advantages in this environment because of the flexibility and characteristic spatial selectivity. The digital beamformer facilitates such things as multi-user spatial processing, operation in a dynamic traffic environment, and ultimately, range and capacity improvement. In the current implementation, the objective is to scan the phased-array in such a way that multiple spatial swaths may be processed in parallel using a real-time FPGA platform. Preliminary results with the PAA have been promising. The results of this effort will be presented in a subsequent article.

6. Conclusion

A smart antenna for cellular PCS has been developed using a digital beamforming approach that digitizes over the entire RF bandwidth using bandpass sampling. The effects of loading the ADC for various SNR scenarios have been shown. These loading issues led to the investigation of AGC approaches that were discussed in this paper. The main conclusion drawn from these AGC approaches is that they are equivalent for the most part with the exception of one having more dynamic range in the presence of co-channel interference. This digital PAA approach will lead to lighter and less expensive systems with more capability and flexibility when compared to current analog PAA technology.

Acknowledgment

The authors would like to thank Dr. Jeff Stocker for the analog-to-digital converter spur-free dynamic-range data.

References

[1] J. C. Liberti, Jr. and T. S. Rappaport, *Smart Antennas for Wireless Communications*, New Jersey: Prentice Hall, 1999.

[2] B. D. Carlson, L. M. Goodman, J. Austin, M. W. Ganz, and L. O. Upton, "An ultralow-sidelobe adaptive array antenna," *The Lincoln Laboratory Journal* , vol. 3, No. 2, pp. 291-310, 1990.

[3] R. G. Vaughan, N. L. Scott, and D. R. White, "The theory of bandpass sampling," *IEEE Trans. Signal Processing*, vol. 39, pp. 1973-1984, Sep. 1991.

[4] R. T. Compton, Jr., *Adaptive Antenna. Concepts and Performance*, Prentice Hall, New Jersey, 1988.

[5] R. Klemn, *Space-Time Adaptive Processing Principles and Applications*, Stevenage, Hertfordshire, United Kingdom: Institute of Electrical Engineers, 1998.

[6] G. A. Gray and G. W. Zeoli, "Quantization and saturation noise due to analog-to-digital conversion," *IEEE Trans. Aerospace and Electronic Systems*, pp. 222-223, Jan. 1971.

[7] Y. Li and N. R. Sollenberger, "Adaptive antenna arrays for OFDM systems with cochannel interference," *IEEE Trans. Communications*, vol. 47, no. 2, pp. 217-229, Feb. 1999.